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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,492	12/31/2003	Narendra Amalendu Soman	134486/068709-046	1807
29391	7590	06/24/2005	EXAMINER	
BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A. 390 NORTH ORANGE AVENUE SUITE 2500 ORLANDO, FL 32801			BHAT, ADITYA S	
			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/750,492	Applicant(s) SOMAN ET AL.	
	Examiner Aditya S. Bhat	Art Unit 2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 11-30 is/are rejected.
- 7) ☒ Claim(s) 9 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/10/04</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 and 11-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Gong et al. (USPUB 2004/0098220).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

With regards to claim 1, Gong et al. (USPUB 2004/0098220) teaches a method for determining a one-dimensional gap stack-up for a gap within an assembly of parts, the method comprising:

identifying a gap for stack-up analysis; (Page 2, Paragraph 0017) (102;

Refer to figure 1)

identifying a first surface and a second surface defining the gap, wherein a first part of the assembly of parts comprises the first surface and a second part of the assembly of parts comprises the second surface; (Page 2, Paragraph 0017) (104; Refer to figure 1) and

determining a vector loop comprising a plurality of elements from the first surface through the assembly of parts to the second surface, wherein the plurality of elements comprise the gap stack-up. (Page 2, Paragraph 0019)

With regards to claim 2, Gong et al. (USPUB 2004/0098220) teaches the vector loop comprises vector loop segments, and wherein the step of determining the vector loop further comprises determining the vector loop segments between geometric planes of the assembly of parts for which a normal to the plane is collinear with the vector loop. (Page 2-3, Paragraph 0020)

With regards to claim 3, Gong et al. (USPUB 2004/0098220) teaches the geometric planes comprise geometric planes between two parts of the assembly of parts. (Page 1, Paragraph 0002)

With regards to claim 4, Gong et al. (USPUB 2004/0098220) teaches the geometric planes comprise geometric planes within a part of the assembly of parts. (Page 1, Paragraph 0002)

With regards to claim 5, Gong et al. (USPUB 2004/0098220) teaches the vector loop comprises vector loop segments, and wherein a dimension is associated with each vector loop segment, and wherein the method further comprises combining the dimension associated with each of the vector loop segments to determine a gap stack-up dimension. (Page 2, Paragraph 0019)

With regards to claim 6, Gong et al. (USPUB 2004/0098220) teaches multiplying each dimension by a weight and summing the resulting products.

(Page 2, Paragraph 0019)

With regards to claim 7, Gong et al. (USPUB 2004/0098220) teaches the weight comprises a numerical value indicating the relationship between a change in the dimension of a vector loop segment and a change in the gap stack-up dimension. . (Page 2, Paragraph 0017)

With regards to claim 8, Gong et al. (USPUB 2004/0098220) teaches the weight comprises a +1 or a -1, and wherein the +1 weight indicates a direct relationship between the change in the dimension of the vector loop segment and the change in the gap suck-up dimension, and wherein a -1 weight indicates an inverse relationship between the change in the dimension of the vector loop segment and the change in the gap stack-up dimension. (Page 2, Paragraph 0017)

With regards to claim 11, Gong et al. (USPUB 2004/0098220) teaches providing a three-dimensional representation of the assembly of parts, wherein the step of identifying the gap filter comprising identifying the gap from the three-dimensional representation. (Page 2, Paragraph 0016)

With regards to claim 12, Gong et al. (USPUB 2004/0098220) teaches providing a three-dimensional representation of the assembly of parts, wherein the step of identifying the first and the second surfaces further comprises identifying the first and the second surfaces from the three-dimensional representation. (Page 2, Paragraph 0017)

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With regards to claim 13, Gong et al. (USPUB 2004/0098220) teaches superimposing a representation of the vector loop on the three-dimensional representation of the assembly of parts. (Page 2, Paragraph 0016)

With regards to claim 14, Gong et al. (USPUB 2004/0098220) teaches the three-dimensional representation comprises a representation provided by a computer-aided design system (Page 4, Paragraph 0029)

With regards to claim 15, Gong et al. (USPUB 2004/0098220) teaches the step of determining the vector loop further comprises determining a plurality of dimensions in the vector loop between the first surface and the second surface. (Page 2, Paragraph 0017)

With regards to claim 16, Gong et al. (USPUB 2004/0098220) teaches each of the plurality of dimensions includes an associated tolerance. (Page 2, Paragraph 0017)

With regards to claim 17, Gong et al. (USPUB 2004/0098220) teaches combining the tolerances to determine the gap tolerance. (Page 4, Paragraph 0027)

With regards to claim 18, Gong et al. (USPUB 2004/0098220) teaches combining further comprises summing the tolerances. (Page 4, Paragraph 0027)

With regards to claim 19, Gong et al. (USPUB 2004/0098220) teaches determining a relationship between each tolerance and a standard deviation for the dimension with which the tolerance is associated; determining the standard deviation for each dimension; and determining the standard deviation of the gap

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according to the root sum of the squares of the standard deviation. (Page 2, Paragraph 0019)

With regards to claim 21, Gong et al. (USPUB 2004/0098220) teaches determining at least one of a dimension and a tolerance for each one of the plurality of elements; and providing a list of each one of the plurality of elements and the at least one of the dimension and the tolerance associated therewith in a spreadsheet format. (Refer to figure 5)

With regards to claim 22, Gong et al. (USPUB 2004/0098220) teaches determining at least one of the gap dimension and the gap tolerance by combining the respective dimension and tolerance of each one of the plurality of elements; and providing the gap tolerance and the gap dimension in the spreadsheet format. (Refer to figure 5)

With regards to claim 23, Gong et al. (USPUB 2004/0098220) teaches the vector loop comprises vector loop segments, and wherein one or more of the vector loop segments comprises a mating pin and hole, wherein an axis of the pin and hole combination is perpendicular to the vector loop. (Page 1, Paragraph 0002)

With regards to claim 24, Gong et al. (USPUB 2004/0098220) teaches a method for determining a vector loop within an assembly of parts comprising:

(a) identifying a loop from-face of a first part and a loop to-face of a second part of the assembly of parts, wherein the vector loop extends there between; (102; Refer to figure 1) and

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(b) identifying parts in contact at a contact face within the assembly of parts, wherein a normal to the contact face is collinear with the vector loop, and wherein each identified part comprises a part from-face and a part to-face, and wherein the vector loop extends from the loop from-face of the first part through the from-face and the to-face of each succeeding part in contact at the contact face, to the loop to-face of the second part. (Page 2, Paragraph 0017)

With regards to claim 25, Gong et al. (USPUB 2004/0098220) teaches for each part identified in the step (b), determining at least one of the dimension and the tolerance between the loop from-face and the loop to-face. (Page 1, Paragraph 0005)

With regards to claim 26, Gong et al. (USPUB 2004/0098220) teaches determining all parts within the assembly of parts; (Page 2, Paragraph 0016)

With regards to claim 28, Gong et al. (USPUB 2004/0098220) teaches a computer program product for performing a one-dimensional gap for a gap within an assembly of parts, the computer program product stack-up comprising:

a storage medium readable by a computer processor and storing program code for execution by the computer processor, the program code comprising:

(Refer to figure 6)

a program code module for identifying a gap for stack-up analysis; (Refer to figure 1)

a program code module for identifying a first surface and a second surface defining the gap, wherein a first part of the assembly of parts comprises the parts

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surface and a second pm of the assembly of parts comprises the second surface;
and (Page 2, Paragraph 0017) (104; Refer to figure 1)

a program code module for determining a vector loop comprising a plurality of elements from the first surface through the assembly of parts to the second surface, wherein the plurality of elements comprise the gap stack-up.
(Page 2, Paragraph 0019)

With regards to claim 29, Gong et al. (USPUB 2004/0098220) teaches a program code module for identifying at least one of a dimension and a tolerance for each one of the plurality of elements.(510; Refer to figure 5)

With regards to claim 30, Gong et al. (USPUB 2004/0098220) teaches a program code module for determining at least one of a mean gap dimension and a standard deviation of the mean dimension in response to the respective dimension and tolerance for each one of the plurality of elements. (Page 1, Paragraph 0005)

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 9-10:

The primary reason for the allowance of claim 9 is the inclusion of the method steps of: a numerical value indicating the relationship between a change in a dimension of vector loop segment caused by a change in at a environmental

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condition to watch the assembly of parts is subjected and a change in the gap stack-up dimension resulting from the change in the environmental condition. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Claim 10 is allowed due to their dependency on claim 9.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Drake et al. (USPUB 2004/0030427) teaches a mechanical tolerance method and Tandler (USPN 6,507,806) teaches a computer aided design (CAD) system for automatically constructing datum reference frame (DRF) and feature control frame (FCF) for machine part.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S. Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

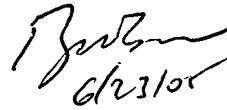
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
June 22, 2005

BRYAN BUI
PRIMARY EXAMINER



6/23/05